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Claims

[c1] 1. A process for fabricating a dynamic random access memory (DRAM), comprising the steps of:
providing a substrate;
forming a plurality of trenches in the substrate;
forming a capacitor inside each trench;
patterning a plurality of active regions on the substrate;
forming a plurality of word lines on the substrate;
forming a pair of source/drain regions in each active region; and
forming a plurality of bit lines over the substrate,
wherein a first side edge of each active region has a first trench whose capacitor is coupled to the active region, furthermore, a second side edge of an adjacent active region has a second trench such that a word line passes through both the active region and the second trench, moreover, the area in the active region covered by the word line serves as a channel region;
the source/drain regions of each active region are electrically connected to a capacitor and a bit line; and
after forming the trenches but before patterning the active regions, further comprises performing an ion implantation tilted at an angle along the word line direction

to form a doped region on each side of the predetermined channel region in the substrate such that the dopants within the doped regions has a conductive type identical to that of the substrate.

[c2] 2. The DRAM process of claim 1, wherein the step of forming a capacitor in each trench comprises:
forming an external electrode in the substrate at a lower section of the trench;
forming a capacitor dielectric layer on the surface of the trench;
depositing a conductive material into the trenches to form a first conductive layer; and
connecting the first conductive layer with a corresponding source/drain region.

[c3] 3. The DRAM process of claim 2, wherein after forming the first conductive layer in the trenches, the DRAM process further comprises:
removing a portion of the first conductive layer above a lower trench section;
forming a collar dielectric layer over a top surface of the lower trench section;
forming a second conductive layer over the first conductive layer such that the second conductive layer is surrounded by the collar dielectric layer; and
connecting the second conductive layer with a corre-

sponding source/drain region.

[c4] 4. The DRAM process of claim 3, wherein the ion implantation is carried out after forming the collar dielectric layer.

[c5] 5. The DRAM process of claim 4, wherein the ion implantation is carried out after forming the collar dielectric layer but before forming the second conductive layer.

[c6] 6. The DRAM process of claim 3, wherein after forming the second conductive layer, the DRAM process further comprises:
forming a third conductive layer over the second conductive layer to provide a direct contact with a corresponding active region, wherein the third conductive layer is constructed using a doped semiconductor material; and
activating the dopants within the third conductive layer to diffuse into the active region and form a buried strap structure for connecting with a corresponding source/drain region.

[c7] 7. The DRAM process of claim 6, wherein a top surface of the third conductive layer is at a level below a top surface of the substrate.

[c8] 8. The DRAM process of claim 7, wherein the ion implan-

tation is carried out after forming the third conductive layer.

[c9] 9. The DRAM process of claim 6, wherein material constituting the first conductive layer, the second conductive layer and the third conductive layer comprises doped polysilicon.

[c10] 10. A process for fabricating a dynamic random access memory (DRAM), the process comprising the steps of:
providing a substrate;
forming a plurality of trenches in the substrate;
forming a capacitor inside each trench;
patterning a plurality of active regions on the substrate;
forming a plurality of word lines running in a first direction over the substrate;
forming a pair of source/drain regions and a common source/drain region in each active region; and
forming a plurality of bit lines running in a second direction over the substrate,
wherein all four side edges of each active region have a pair of trenches such that the capacitor in one of the trenches in each pair of trenches along the second direction is coupled to the active region and the capacitors in the pair of trenches along the first direction are coupled to other active regions, furthermore, a pair of adjacent word lines passes through the active region and the two

pairs of trenches along the first direction, moreover, the areas in the active region covered by the two word lines serve as two channel regions;

each of the two source/drain regions within each active region is electrically connected to a capacitor and the common source/drain region is electrically connected to a bit line; and

after forming the trenches but before patterning the active regions, the process further comprises performing an ion implantation tilted at an angle along the first direction to form four doped regions on each side of the predetermined two channel regions in the substrate such that the dopants within the doped regions has a conductive type identical to the substrate.

[c11] 11. The DRAM process of claim 10, wherein the step of forming a capacitor in each trench comprises:

forming an external electrode in the substrate at a lower section of the trench;

forming a capacitor dielectric layer on the surface of the trench;

depositing a conductive material into the trenches to form a first conductive layer; and

connecting the first conductive layer with a corresponding source/drain region.

[c12] 12. The DRAM process of claim 11, wherein after forming the first conductive layer in the trenches, the DRAM process further comprises:
removing a portion of the first conductive layer above a lower trench section;
forming a collar dielectric layer over a top surface of the lower trench section;
forming a second conductive layer over the first conductive layer such that the second conductive layer is surrounded by the collar dielectric layer; and
connecting the second conductive layer with a corresponding source/drain region.

[c13] 13. The DRAM process of claim 12, wherein the ion implantation is carried out after forming the collar dielectric layer.

[c14] 14. The DRAM process of claim 13, wherein the ion implantation is carried out after forming the collar dielectric layer but before forming the second conductive layer.

[c15] 15. The DRAM process of claim 12, wherein after forming the second conductive layer, the DRAM process further comprises:
forming a third conductive layer over the second conductive layer to provide a direct contact with a corre-

sponding active region, wherein the third conductive layer is constructed using a doped semiconductor material; and

activating the dopants within the third conductive layer to diffuse into the active region and form a buried strap structure for connecting with a corresponding source/drain region.

[c16] 16. The DRAM process of claim 15, wherein a top surface of the third conductive layer is at a level below a top surface of the substrate.

[c17] 17. The DRAM process of claim 16, wherein the ion implantation is carried out after forming the third conductive layer.

[c18] 18. The DRAM process of claim 15, wherein material constituting the first conductive layer, the second conductive layer and the third conductive layer comprises doped polysilicon.

[c19] 19. A dynamic random access memory (DRAM) structure, comprising:

a substrate with a trench;

a capacitor formed inside the trench;

an active region surrounded by an isolation region formed over the substrate;

a word line formed over the substrate and passed through the active region, wherein an area in the active region covered by the word line serves as a channel region;

a pair of source/drain regions within the active region formed on each side of the word line such that the source/drain regions connect with the capacitor and a bit line respectively; and

a doped region with dopants in a conductive type identical to that of the substrate formed on each side of the channel regionadjacent to the isolation region.

[c20] 20. The DRAM structure of claim 19, wherein the capacitor inside the trench comprises:

an external electrode in the substrate formed at a lower section of the trench;

a capacitor dielectric layer formed on the surface of the trench; and

a first conductive layer formed inside the trench and electrically connected to a corresponding source/drain region.

[c21] 21. The DRAM structure of claim 20, wherein the capacitor further comprises:

a collar dielectric layer formed on the sidewall above the first conductive layer; and

a second conductive layer formed over the first conduc-

tive layer surrounded by the collar dielectric layer such that the first conductive layer connects electrically with a corresponding source/drain region through the first conductive layer.

[c22] 22. The DRAM structure of claim 21, wherein the capacitor further comprises a third conductive layer and a buried strap such that the third conductive layer is formed over the collar dielectric layer and the second conductive layer and is electrically connected to a corresponding source/drain region through the buried strap.

[c23] 23. The DRAM structure of claim 22, wherein the third conductive layer has a top surface below a top surface of the substrate.

[c24] 24. A dynamic random access memory (DRAM) structure, comprising:
a substrate with a plurality of trenches;
a capacitor formed within each trench;
a plurality of active regions surround by an isolation region formed over the substrate;
a plurality of word lines running in a first direction formed over the substrate;
a plurality of source/drain regions and a plurality of common source/drain regions formed within various active regions such that a pair of source/drain region and a

common source/drain region together form a group inside each active region;
a plurality of bit lines running in a second direction formed over the substrate; and
a plurality of doped regions formed in the substrate such that dopants inside the doped region has a conductive type identical to that of the substrate,
wherein all four side edges of each active region have a pair of trenches such that the capacitor in one of the trenches in each pair of trenches along the second direction is coupled to the active region and the capacitors in the pair of trenches along the first direction are coupled to other active regions,
a pair of adjacent word lines passes through the active region and the two pairs of trenches along the first direction and the areas in the active region covered by the word lines serve as two channel regions, moreover, the doped regions are formed on each side of each channel region adjacent to the isolation region, and
each source/drain region within each active region is electrically connected to a capacitor and the common source/drain region is electrically connected to a bit line.

[c25] 25. The DRAM structure of claim 24, wherein the capacitor inside the trench comprises:
an external electrode in the substrate formed at a lower

section of the trench;
a capacitor dielectric layer formed on the surface of the trench; and
a first conductive layer formed inside the trench and electrically connected to a corresponding source/drain region.

[c26] 26. The DRAM structure of claim 25, wherein the capacitor further comprises:
a collar dielectric layer formed on the sidewall of the trench above the first conductive layer; and
a second conductive layer formed over the first conductive layer surrounded by the collar dielectric layer such that the first conductive layer connects electrically with a corresponding source/drain region through the first conductive layer.

[c27] 27. The DRAM structure of claim 26, wherein the capacitor further comprises a third conductive layer and a buried strap such that the third conductive layer is formed over the collar dielectric layer and the second conductive layer and is electrically connected to a corresponding source/drain region through the buried strap.

[c28] 28. The DRAM structure of claim 27, wherein the third conductive layer has a top surface below a top surface of the substrate.